Please cancel claim 1.

2. (As amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

[The method of claim 1 further comprising the steps of:]

forming a first memory gate electrode on said second oxide layer thickness, said second oxide layer thickness formed on said semiconductor substrate in a memory region.

3. (As amended herein) The method of claim 2 wherein introducing said halogen-containing impurities **[introducing step]** comprises **[the step of]**:

masking a **[said]** dielectric layer to expose said first region, said dielectric layer formed on said substrate; and

wherein said halogen-containing impurities are introduced through said dielectric layer to said first region.

4. (As amended herein) The method of claim 2 **[3]** wherein introducing said halogen-containing impurities **[introducing step]** comprises an ion implantation.

5. (As amended herein) The method of claim 2 **[1]** wherein introducing said halogen-containing impurities **[introducing step]** comprises **[the step of]** introducing halogen-containing impurities into said first region and wherein said second region has substantially no halogen concentration therein.

6. (As amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

[The method of claim 1] wherein introducing said halogen-containing impurities **[introducing step]** comprises **[the steps of]** introducing halogen-containing impurities into said first region at a first concentration and introducing halogen-containing impurities into said second region at a second concentration, said first concentration greater than said second concentration.

7. (As amended herein) The method of claim 6 **[5]** wherein introducing said halogen-containing impurities **[introducing step]** comprises an ion implantation.

8. (As amended herein) The method of claim 2 **[1]** wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

9. (As amended herein) The method of claim 2 **[1]** wherein said semiconductor substrate also includes a third region where a third oxide layer thickness is desired, and wherein introducing said halogen-containing impurities **[introducing step]** also introduces halogen-containing impurities such that a different halogen concentration is formed in said third region than in said first region and **[or]** in said second region.

10. (As amended herein) The method of claim 2 **[1]** wherein said semiconductor device comprises a flash EEPROM semiconductor device.

11. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a floating gate electrode.

12. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a stack gate cell.

13. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a split gate cell.

14. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a control gate electrode.

15. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a stack gate cell.

16. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a split gate cell.

Please cancel claims 17-19.

20. (As amended herein) A method of forming a semiconductor integrated circuit, said method comprising **[steps of]**:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities through said gate dielectric layer and into said second region; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process.**[;]**

Support (Fig. 3D) (p. 23-25)

Support (Fig. 3B)

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wherein said first thickness is sufficiently thin to provide high driving capability for said MOS transistor, and said second thickness is sufficiently thick to provide high voltage reliability of said high voltage device.]

21. (As amended herein) A method of forming a semiconductor integrated circuit, said method comprising:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities into said second region; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process;

[The method of claim 20] wherein said **[step of]** selectively implanting halogen-containing impurities into said first region also includes selectively implanting halogen-containing impurities into said second region such that said first region has a greater halogen concentration than said second region.

22. (As filed) The method of claim 20 wherein said halogen containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

23 (As filed) The method of claim 20 further comprising forming a third thickness of dielectric material overlying a third region, said third region being spatially apart from said first region and said second region.

Please add the following claims:

--24. A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired;

forming a dielectric layer on said substrate;

masking said dielectric layer to expose said first region;

introducing a halogen-containing impurities through said dielectric layer and into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.

25. The method of claim 24 wherein said introducing said halogen-containing impurities comprises an ion implantation.

26. The method of claim 24 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

27. A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired, a second region where a second oxide layer thickness is desired, and a third region where a third oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region, and a different halogen concentration in said third region than in said first region and said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.

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Cont

28. The method of claim 27 wherein said performing an oxidizing process also simultaneously forms said third oxide layer thickness at said third region.—

REMARKS

Claims 1-17 and 20-23 were examined. Claims 2-10, 20 and 21 have been amended. Claims 1 and 17-19 have been canceled, and claims 24-28 have been added. Reconsideration of the subject application as amended is respectfully requested.

Claims 2 and 6 have been indicated by the Examiner as allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Claims 3, 4, 9, 11-16 and 21 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, and have been indicated by the Examiner as allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. §112, 2nd paragraph and to include all the limitations of the base claim.

Claims 1, 5, 7, 8, 10, 17, 20, 22 and 23 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Takagi.

Claim 17 has been rejected under 37 CFR 1.75(c) as being of improper dependent form.

Claims 20-23 have been rejected under 35 U.S.C. §112, first paragraph.

Applicant respectfully traverses the rejections to claims 1 and 17, but to expedite prosecution has canceled claims 1 and 17 for later filing in a continuation application. Additionally, Applicant has canceled claims 18 and 19 in response to the previously-issued restriction requirement and for later filing in a continuation or divisional application.

CLAIM REJECTIONS UNDER 35 U.S.C. § 112

Appropriate claim amendments have been made, rendering moot the Examiner's rejections under 35 U.S.C. § 112, second paragraph, of claims 3, 4, 9, 11-16 and 21. For example, claim 3 has been amended to provide a proper antecedent basis for the